Remarks:

It is submitted, the changes presented hereinabove together with the supportive discussion/rebuttal arguments provided herein render the application allowable and, therefore, acceptance/formal entry of this Amendment is respectfully requested.

With the above amendments, claims 1-27, 30 and 31 remain pending in this application, of which claims 1-4, 15-17, 20, 23, 26-27 and 30 are currently amended. (Claim 22 remains withdrawn and claims 28-29 were earlier canceled.)

Each of the independent claims was amended to highlight that the surface of the wiring substrate of the semiconductor module on which the semiconductor device is mounted is planar, that is, it is a flat surface, consistent with that shown in the various disclosed embodiments of the present application (e.g., see Figs. 1-2, 6-7, 11, 16-33, etc.), although not limited thereto. This change, also, further highlights the defining aspects of the present invention over that previously known including over the applied art, as cited in the outstanding rejections.

Additionally, claims 3, 4 and 20 were amended in a manner which avoids the "product-by-process" concerns raised in the outstanding Office Action. It is submitted, the language now positively sets forth that the insulating resin layer (e.g., 10, etc.) has a shape defined by a printed pattern. Also in claim 4, the term "board" in the last line thereof was revised to avoid any possible confusion with the similar term "board" recited earlier in that claim. The "board" to which the semiconductor module is mounted on relates to an external substrate such as external board 15 in Fig. 28 of the drawings (see also Figs. 16-19 and 27, etc.). With regard to claim 23, the expression "a board" was revised to <u>said external</u>

substrate, consistent with the related expression in the preamble in that claim. With regard to claim 30, the term "board" in the "wherein" clause thereof was appropriately amended to wafer board, similarly as that effected with regard to claim 4, namely, to avoid confusion with the similar term "board" set forth earlier in that claim.

Claim 26 was additionally amended to effect further clarification of the subject matter intended to be covered including in terms of avoiding any previously outstanding concern such as that discussed in item 7 on page 4 of the outstanding Office Action. Specifically, independent claim 26 was further amended in the manner which clearly sets forth a semiconductor module scheme such as that shown in Figs. 21-22 of the drawings (although not limited thereto) which has a reduced area coverage by disposing the wiring and the electrode connected thereto on the insulating material (the external connection terminals or bumps 5 are disposed above the rear surface of the flip-chip mounted semiconductor devices 1 in Figs. 21-22). Accordingly, in view of the clarifying revisions being implemented to claim 26, any and all previously outstanding question(s) of definiteness were rendered moot. Therefore, insofar as presently applicable, the rejection of claims 26 and 27 under 35 USC §112, second paragraph, is traversed and reconsideration and withdrawal of the same is respectfully requested.

According to the outstanding Final Office Action, claims 1, 2, 5-8, 10-14, 24, 26, 27, 30 and 31, "insofar as definite," were rejected under 35 USC §103(a) over the combination of Launay (USP 6,320,753) in view of Yukawa (USP 6,436,733); claims 3 and 4, "insofar as definite," were rejected under 35 USC §103(a) over the combination of Launay and Yukawa, as applied to claim 1, and

further in view of Shoji (USP 6,054,171); claim 9 was rejected under 35 USC §103(a) over Launay and Yukawa, as applied to claim 1, and further in view of Hembree (USP 6,242,932); claims 15-19, 21 and 25 were rejected under 35 USC §103(a) over the same combination of Launay and Yukawa, as applied to claims 1-2, and further in view of Lee (USP 5,986,334); and claim 20 was rejected under 35 USC §103(a) over the combination of Launay, Yukawa and Lee, as applied to claims 1 and 16, and further in view of Shoji (*supra*). It will be shown, hereinbelow, the invention according to these claims, as now amended, could not have been realized in a manner as that alleged in the outstanding rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

In independent claim 1, the semiconductor module set forth therein features a semiconductor device and a wiring substrate in which the semiconductor device is mounted on a planar surface on a principle side of the wiring substrate and further calls for an "insulating resin layer" which has an external connection terminal (e.g., bump 5) thereon, the insulating resin layer acting as a stress relaxing layer between the semiconductor module and a board to which the module is mounted (e.g., in Fig. 1, low elastic modulus layer 10, which is frame-shaped, acts as a stress compliant layer). Similar such featured aspects, although presented in a somewhat modified form therefrom, are also set forth with regard to other ones of the independent claims.

In independent claim 2, further, the set forth "insulating resin layer," which acts as a stress relaxing layer, has both an inclined portion as well as a flat portion, the latter on which the external connection terminal is arranged, and a part of the wiring electrically connected between a terminal on the semiconductor

device and the external connection terminal of the module is formed on the inclined portion of the insulating resin layer. This can be seen in Fig. 1 of the drawings, for example, which shows wiring connections between the external connection terminal 5 on the flat surface of the insulating resin layer 10 and the terminals 6 on the semiconductor device 1, the wirings including portions extended over the inclined portion of the insulating resin layer 10. Fig. 8F shows an example of the formation of wires 3 over the inclined plane surface such as it relates to, for example, independent claim 4, and the shaping/patterning of the insulating resin layer which performs a stress relaxing function is effected in the manner such as that discussed in connection with Figs. 10A-10B, 12 and 35, the latter showing one example of the collective printing of the plural insulating layers on the wafer board.

Independent claim 15, 16 and 17 call for a scheme in which, among other featured aspects thereof, the semiconductor device (e.g., chip or chips) and the wiring substrate mutually are connected via a bump of the semiconductor device. As in other independent claims, the semiconductor module according to claim 15 calls for an insulating resin layer acting as a stress relaxing layer and also calls for the wiring substrate to be a silicon substrate. An example of this is shown in Fig. 29 of the drawings, in which 2 is a silicon substrate. Fig. 30 of the drawings shows a similar scheme but in which the wiring substrate 2 is a glass substrate instead (see claim 9). It is noted that in claim 16 as well as with regard to claim 17, the connection between the semiconductor device (chip/chips) and the wiring substrate is effected without the need of an underfill. In independent claim 17, the invention further calls for a "first insulating resin layer" which relieves stress between the semiconductor module and a board to which the module is mounted

and a "second insulating resin layer" which relieves stress between the chip and the wiring substrate. Fig. 30, although not limited thereto, is an example showing of such featured aspects.

Independent claim 23 further calls for, among other aspects thereof, the placement of a heat conductive material layer on the external substrate to which the semiconductor module is mounted (e.g., see Figs. 16 and 17). With regard to independent claim 30, the invention set forth therein also calls for an "insulating resin layer" which acts as a stress relaxing layer between the semiconductor module and the board to which the module is mounted. More particularly, the "insulating resin layer" in claim 30 represents one of plural such insulating resin layers that are collectively molded on a wafer board including plural wiring substrates. Moreover, according to claim 30 and, also, in claim 1 as well as in other claims, the insulating resin layer has a thickness greater than the semiconductor device, an example description of which is found on page 62 of the Substitute Specification, beginning in paragraph [0208]. Additional related discussion is found from page 20 to page 24 of the Substitute Specification regarding implementing the thickness of the stress relaxing layer and its relationship to the module itself. The dependent claims also cover various details regarding the semiconductor module of the present invention. It is submitted, the invention according to claims 1+, 2+, 4, 15, 16+, 17, 23, 26+ and 30+ could not have been attainable from the combined teachings of the cited references, as applied in the respective rejections. Each of the art rejections will now be addressed.

I. *Rejection of Claims 1, 2, 5-8, 10-14, 24, 26, 27, 30 and 31 over the combination of Launay in view of Yukawa.*

Contrary to that alleged in the rejection, wiring 15 of Launay is not disposed on the support (wiring substrate) 2 but, rather, is disposed on the slant portion of the strip layer 3 such as can be seen from Figs. 3-6 of the drawings, etc. The wiring disposed on the substrate 2 is the antenna wiring 10. As can be seen from Fig. 5 of the drawings, for example, in Launay, reference 9 represents connection terminals and 5 are the connection ends of the insulated circuit (chip) 1. Also, contrary to the assertions made on page 6 of the outstanding Office Action, the pad of the wiring 15 is not formed on the inclined portion of the insulating strip layer 3; rather, wiring 15 is disposed on the inclined portion of the strip layer 3.

It is also noted that the insulating strip layer 3 of Launay is not provided at a circumferential/peripheral portion of the substrate in contradistinction with that in Figs. 1+, 6+, etc. of the example disclosed embodiments of the present application, although not limited thereto. With regard to the sectional view shown in Fig. 7 of the drawings of the present application, it is noted that the insulating resin layer 10 has an inclination at an inner circumferential side that rises relatively more gradually than that of an outer circumferential side thereof. An example discussion of this is given with regard to Figs. 8E-8F of the drawings in the present application. The opening or cavity portion according to Launay's scheme, which contains the integrated circuit 1 and connection terminals thereof, represents an opening such as that shown in Figs. 1 and 10 thereof, in which with regard to Fig. 1, a protective resin coating 18 is also provided thereon. That is, the actual arrangements associated with Figs. 4 and 5 are not commensurate with that shown in Figs. 1+, 6+, etc., of the present application, which are example

showings thereof of the present invention, in which the insulating resin layer 10 is disposed as a circumferential portion of the substrate.

Moreover, each of the independent claims now also calls for the entire principle surface of the wiring substrate (on which the semiconductor device is mounted) to be planar (i.e., a flat surface). However, as can be seen from the various example embodiments shown in Launay, a required aspect thereof is that the antenna wirings 10, underlying the integrated circuit 1 in the cavity, be provided on a surface of the support 2 that is recessed from the principle side thereof. It is noted that according to Launay's teachings, the board which includes the integrated circuit 1, the support substrate 2, the insulating strip layer 3 and the cavity 4 must have an upper surface that is defined by the upper surface of the strip layer 3. This can be seen from a careful viewing of the example showings in Figs. 4, 5, 15 and 16 in Launay. With regard to Figs. 20 and 21 thereof, a relatively thick insulating strip layer 3 is not shown. In accordance with Launay's example showings in Figs. 26 and 27, further, it is observed that the integrated circuits 1 are not mounted on the principle surface of the support 2 as would be required according to the present invention, along with other differences therebetween. It is also noted that the antenna (constituting the wirings on the substrate) is embedded in a cavity in the support substrate 2 underlying the integrated circuit 1 in Figs. 26 and 27 in Launay.

Launay's scheme calls for external connecting terminals that are, in effect, contact shoes (i.e., external contact zones). The present invention, on the other hand, was implemented to be suitable for a semiconductor module employing bumps as external connection terminals. If, therefore, a bump structure is employed with regard to Launay's construction, problems would arise. For one,

the presence of bump electrodes would cause abrasion at the tips and, also, would lead to cracks at the root of the bumps. In other words, the teachings in Launay's disclosure limits the external connection terminals to flat external pads without bumps (i.e., without protruding conductors). Otherwise, Launay's construction would become defective.

The wiring substrate according to the present invention, in contradistinction to that taught by Launay, has a flat principle surface and has a coefficient of expansion which is closer to the coefficient of linear expansion of the semiconductor device. The present inventors have schemed a semiconductor module that utilizes a wiring substrate, which may be made of silicon, ceramic or glass, having a coefficient of expansion which is closer to the coefficient of linear expansion of the semiconductor device (chip) so as to effect a reliable flip-chip connection to the wiring substrate. (A flip-chip connection connects the front face of the chip, where the integrated circuit is formed as well as where the external contacts of the chip are provided, to the base (or wiring) substrate.)

It is alleged that Launay as combined with Yukawa's teachings of using thermoplastic material would have led one of ordinary skill to consider the insulating strip layer 3 of Launay as a stress relaxing layer in the manner as that called for in each of the independent claims. However, such could not have been realized therefrom noting that usage of the material, purpose, the way the respective insulating layers are applied, the operation associated therewith and the effects realized are completely different between that taught in Yukawa and that taught by Launay.

Yukawa, it is submitted, disclosed a resin-based thermoplastic composite layer 12 which includes a thermo-plastic film bonding layer 12a and a paste-based

bonding layer 12b (see Fig. 1). The layer 12 acts as a bonding layer between the radiator plate 10 and the chip 14. Launay, on the other hand, disclosed a scheme in which the insulating strip 3 (formed of thermoplastic material) is provided between the antenna and the external connection terminals (external contact zones). (Column 1, lines 45-48, in Launay.) It is clearly apparent therefore that the resin-based thermoplastic material of Yukawa is implemented differently and is employed for a totally different purpose from that taught by Launay. Bonding is a characteristic whose purpose is to effect a joining between different parts such as between the rear surface of the chip 14 and the radiator plate 10 in Fig. 1 of Yukawa. On the other hand, the insulating characteristics associated with the insulating strip layer 3 in Launay is to effect electrical isolation. It is clearly apparent therefor that both the strategic placement as well as operation and effects are in total conflict between that taught by the composite bonding layer 12 of Yukawa and the insulating strip layer 3 of Launay. It is submitted, therefore, that one of ordinary skill would not have thought of electrical insulation characteristics from the bonding considerations associated with composite layer 12 of Yukawa.

Further, it is noted that while the integrated circuit 1 of Launay is disposed face-down in the cavity, the semiconductor chip 14 of Yukawa is rear surface bonded to the radiator plate. According to this, it is noted that the bonding material according to Yukawa is disposed between the rear surface of the chip and the radiator plate while the insulator strip layer 3 is disposed outside the plan view area of the chip. It is submitted, therefore, one of ordinary skill would not have been led to compose an insulating resin layer, as called for in the present invention, in view of the teachings of strictly using a resin-based composite layer

as a bonding agent, according to Yukawa.

For at least the above reasons, the invention according to claims 1, 2, 5-8, 10-14, 24, 26, 27, 30 and 31 could not have been realized from the combined teachings of Launay and Yukawa. As to the particularly featured aspects called for in claims 6 and 7, they are also defining even over the combined teachings of Launay and Yukawa. Dependent claim 6 further calls for the insulating resin layer to be frame-shaped such as shown in Figs. 1, 6, etc., in the present application. From Figs. 1 and 10 of Launay, however, the shape of strip layer 3 is clearly not a frame-shape. Also, insofar as applicable to the featured aspects according to dependent claim 7, the gradient of an outer circumferential side of the strip layer 3 from Fig. 10 of Launay, it is submitted, does not appear to be ascertainable. It is further asserted that it would have been obvious to "have a plurality of insulating resin layers instead of one insulating layer ...," such as set forth in claim 8, and so forth. However, as described in the Specification in connection with the showings in Fig. 17 of the drawings, for example, one of the reasons for dividing the insulating layer 3 into plural layer portions is to promote ventilation for purposes of heat dissipation. In contradistinction with this, Launay neither disclosed nor even hinted at providing ventilation for purposes of heat dissipation. Therefore, the further aspects featured in claim 8, etc., could not have been realized in the manner as that alleged. For these and other reasons, the invention according to claims 1, 2, 5-8, 10-14, 24 (including claim 23), 26, 27, 30 and 31 could not have been rendered obvious from the combined teachings of Launay and Yukawa. Even though independent claim 23 was not specifically included in any of the set forth rejections, the supportive discussion/rebuttal arguments presented herein are also applicable to this claim. It is submitted, therefore, claim 23 should also

be rendered allowable.

II. *Rejection of Claims 3 and 4 over the combination of Launay, Yukawa and Shoji.*

The above supportive discussion in favor of patentability including the rebuttal arguments to the rejection based on Launay in view of Yukawa are also applicable herein. Further, the previously used "product-by-process" concerns are no longer at issue in view of the amendments made to these claims.

It is admitted in the rejection of claims 3 ands 4 that Launay-Yukawa both failed to disclose forming the insulating resin layer by mask printing. Shoji was applied as, allegedly, teaching a technique to precisely control the thickness of the resin. However, these references, even when considered combinedly, did not teach controlling the shape of the insulating resin layer in accordance with a printed pattern scheme, an example of which is shown in connection with Figs. 10A-10B and 12 of the present application. It is submitted, therefore, for the same and similar reasons as that argued above in connection with claims 1, etc., and in view of the additional discussion herein, the invention according to claims 3 and 4 could not have been realized from the combined teachings of Launay-Yukawa in view of Shoji.

III. *Rejection of Claim 9 over Launay-Yukawa and further in view of Hembree.*

The supportive discussion and rebuttal arguments provided under Section I, above, are also applicable herein. In this regard, it is noted that Hembree was strictly cited for its showing that a substrate such as interconnect substrate 56 can

be a glass substrate. However, the construction taught by Hembree, which is directed to an interposer for semiconductor devices, does not overcome the deficiencies earlier discussed in these remarks regarding the combined teachings of Launay and Yukawa, insofar as the present invention is concerned. Hembree, it is submitted, neither disclosed nor even hinted at using glass or silicon material of a flat surface in a construction scheme as that presently called for in claim 9 (as combined with claim 1), which facilitates fine wiring formation including the interconnection between the semiconductor device and external circuitry to the module via the fine wiring. It is submitted, for at least the same reasons presented in Section I, above, as supplemented herein, the invention according to claim 9 (dependent on claim 1) is also considered patentable.

IV. *Rejection of Claims 15-19, 21 and 25 over the combination of Launay-Yukawa and further in view of Lee.*

Launay-Yukawa were applied similarly as that according to claims 1 and 2. Therefore, since these claims are also inclusive of the main featured aspects called for in claims 1+, such as discussed hereinabove, the supportive discussion in favor of patentability including the rebuttal arguments presented hereinabove regarding the applicability of Launay in view of Yukawa, are also applicable herein. As earlier stated, the present invention features a wiring substrate (e.g., made of silicon, ceramic or glass) which has wiring disposed thereon and has a coefficient of expansion which is closer to the coefficient of linear expansion of the semiconductor device so as to support a flip-chip connection capability which can be reliably effected without using an underfill (see Figs. 29, 30, etc.).

Lee disclosed mounting a semiconductor device on a wiring substrate

without using an underfill. However, Figs. 1A, 1C, 2 and 3 in Lee, which were referred to in the rejection, do not show a flip-chip connection that does not require underfill, such as that required according to the present invention. Lee simply disclosed a non-flip-chip scheme without use of underfill.

As to the invention according to claim 25 (dependent on base claim 1), an example of which is shown with regard to Fig. 19 of the present application, in which the semiconductor device is die-attached to module 2, thereby enabling heat dissipation via the module substrate 2. As can be seen from the Fig. 19 example illustration, consistent with that called for in base claim 1, the principle side of the substrate 2 on which the semiconductor device 15 is mounted on is planar over its entirety and, further, the frame-shaped insulating layer 10 has a thickness, consistent with that presently set forth, which is in clear contradistinction with the type of construction afforded the substrate 20 in Lee as well as regarding the multi-layer insulator 26 thereof. Therefore, for the same and similar reasons as that argued with regard to the rejection of claim 1 in Section I, above, and as supplemented herein, the invention according to claim 25 (dependent on claim 1) is also considered patentable. That is, since Lee taught a scheme whose construction is completely different from that of Yukawa and Launay, and since Lee, as just noted, did not overcome the deficiencies in the combined teachings of Launay and Yukawa, insofar as the claims are concerned, the invention according to claims 15-19, 21 and 25 could not have been achievable even over their combined teachings.

V. ***Rejection of Claim 20 over the combined teachings of Launay-Yukawa and Lee and further in view of Shoji.***

Launay-Yukawa and Lee were applied as in the rejection of claims 1 and 16 and, moreover, Shoji was also applied similarly as that with regard to claims 3 and 4. Therefore, the same and similar reasons as that applied in favor of patentability of claims 1, 3-4 and 16, are also applicable herein.

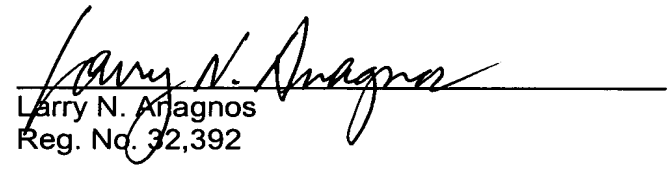
For the above and other reasons, the invention as called for in claims 1+, 2+, 4, 15, 16+, 17, 23+, 26+ and 30+ could not have been rendered obvious in the manner as that alleged in the outstanding rejections. Therefore, since the above amendments together with these accompanying remarks render the above listed claims allowable, acceptance and formal entry therefor of this Amendment as well as a favorable action on the presently pending claims 1-21, 23-27, 30 and 31 and an early formal notification of allowability are respectfully requested.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

If the Examiner does not consider the application allowable at this time, he is requested to enter this amendment and also issue a new Final Office Action which also includes the disposition of claim 23. In this regard the Examiner is directed to the "Request for Complete Office Action ...," filed on December 2, 2003.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40506X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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